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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,313	03/05/2002	Masayuki Ito	TAMA.0003	2895

7590 08/26/2004

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,313	ITO ET AL.	
	Examiner	Art Unit	
	Shane M Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kundu et al. (U.S. Patent No. 5,715,476) in view of Ryan (U.S. Patent No. 6,405,280).

As per claims 1, 4, 5 and 9, Kundu shows a data processing system in figure 1 comprising a CPU 101, a cache 104, and a memory control 108 accessible to a memory 109. The examiner is considering the cache control part to be comprised in the cache 104. Further the examiner is considering the combination of the processor 101, the cache 104, and the memory control 108 to be a --data processing device--. The main memory 109 is comprised of a plurality of memories (SDRAM modules) 201-203 as shown in figure 2. --First information-- for indicating a burst length is contained in register 212 in the cache/memory control 108, more specifically in the smart increment control logic 117. The burst length is also stored in the mode registers 201A-203A of the SDRAM modules (column 8, lines 13-14). The burst length of the memory device can be divisible by consecutive powers of 2, thus yielding a burst length range of 1,2,4,or 8 words as described in column 5, lines 38-40.

Figure 3 shows the data addresses associated with different burst lengths. Because the burst length is configurable (column 5, lines 38-39) and a cache line is a constant size, single or multiple bursts are required to fill a cache line. The examiner is considering a single burst operation to fill the cache line according to figures 3A-3C. As can be seen by the figures, the starting address of the cache miss is the starting address of the data arrangement. For example, in figure 3C, if the 4th block in the cache line is the result of a cache miss (mishit), and the fill line returns with the 4th block of the line. Data following the address of the miss in the line fill are arranged in linear order. The address of the 5th block comes after the 4th block and so on. In addition, if the starting block address (cache miss address) is not the beginning block of the cache line (block address 0), the address --wraps-around-- when being fetched from memory. The first block address (address 0) is arranged after the last block address in the cache line (address 7) as seen in figure 3C.

Kundu does not *specifically* show the arranging of data in the order of addresses according to the --first information-- to corresponding locations in said one of the cache lines independently whether the starting address is a top address of said one of the cache lines or not. Ryan teaches a DRAM burst system that supports a plurality of orderings for data blocks that are fetched from a DRAM memory when requested by a processor during a cache miss (abstract). Similarly, Ryan shows a burst sequence identical to that of Kundu also teaches a --first information-- similar to Kundu as well in column 4, lines 37-38, which includes a starting address and a desired data ordering (including a burst length). Once this request is received by the DRAM controller 150 (figure 5), a data block is sent to the collector 140 and then to cache 120 (column 4, lines 46-53). Ryan shows in figure 3 that different starting address can occur in a

burst sequence (column 300). The starting address is sent in the request packet (first information) from processor 110 as stated above. As taught in column 5, line 60 - column 6 of Ryan, line 5, the order of the data blocks transferred from the DRAM to the collector 140 is unimportant. However, when the data blocks are transferred back to the cache 120, the order of the data blocks must match the order requested by the processor (column 6, lines 6-32). Therefore, the *data is arranged* (by the collector 140) by the order of the request from the processor in order to maintain coherency between the DRAM memory and the cache memory (column 5, lines 60-62). For example, it could have been seen by one having ordinary skill in the art that if the processor requested a sequential burst access starting with '2' as the start address, the processor would have received the data from the DRAM corresponding to the address '2,' followed by the data corresponding to the data from the DRAM corresponding to address '3,' etc. since the ordering of the data is critical (column 6, lines 7-9). The ordering is critical since coherency would be damaged if, for instance, the data of the address '2' was incorrectly sent to the cache as the data for address '0.' In other words, *independent of whether the starting address is the --top-- (or beginning address) of a cache line*, it could have been seen that the data corresponding to the respective address would be correctly input into the cache line *regardless* of when that address [of DRAM] were accessed. Said different in reference to figure 3, column 300, the data associated with address '2' would be the same data regardless as to whether the address '2' was accessed first (starting address = '2') or whether it was accessed last (address = '3'). Thus, Ryan teaches the last two lines of claims 1, 4, 5, and 9.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the burst line fill system of Kunda with the teaching of

a collector of Ryan in order to have maintained memory coherency between a RAM and the cache by ordering the data, corresponding to the requested address sent from the processor to the RAM as a result of a cache mishit, in the proper order that was request by the processor (column 6, lines 6-9, of Ryan), even when that order begins with an address that is not the top address (address = '0') of the cache line that was mishit.

Claims 2,6,7,10,12,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunda et al. (U.S. Patent No. 5,715,476) in view of Ryan (U.S. Patent No. 6,405,280) in further view of Gaskins et al. (U.S. Patent No. 6,081,853), as applied to claims 1,4,5, and 9 above.

As per claims 2,6,7,10,12, and 13 and as discussed above in the rejection for claims 1,4,5, and 9, modified Kunda shows a cache in the data processing device of figure 1; however, specific detail of the cache and its interaction with the memory, as are well know in that art, are not discussed in detail. Therefore the examiner is incorporating the cache system shown in figure 2 of Gaskins to further illustrate the cache memory 104 of modified Kunda. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the cache of the data processing device of modified Kunda with the cache memory shown in figure 2 of Gaskins because the cache memory of Gaskins is a prior art cache for use with burst operations from a main memory (refer to column 4, lines 36-37 of Gaskins). Figures 2 and 3 and column 8, lines 18-28, of Gaskins refer to the common operation of a cache miss and line fill operation. Address information is sent to the memory on where to fetch the data. The cache memory 104 (figure 1) of modified Kunda interacts with the memory control 108 (Kunda) so it is inherent that the cache know how much data (i.e. a full cache line in this case) is returning

from main memory 109 via –sharing—of the information contained in the burst length register 212 of the memory control. Further it is necessarily inherent that this process occur so that cache always receive valid data from the main memory (in other words the cache would not receive 4 words and it was expecting 8 words). The examiner is considering the –address information— received to the cache controller (240 of Gaskins) to be the ADDR lines of figure 3. As can be seen by figures 3 and 5, the address lines contain address information regarding the first address of the burst and then, since the data processing device of modified Kunda could have received address data starting from the address in the cache line that caused the miss as described above, the cache control can then accept the data returned from the memory such as shown on the data lines in figure 5 of Gaskins. The examiner is further considering the –synchronization—signal received by the cache control (240 of Gaskins) to be the ADS# signal since valid data is returned in sync to when the ADS# signal transitions from logic 0 to logic 1. The examiner is considering the cache fill address to be the address of the cache line where the data returned from the main memory is to be stored (i.e. lines 262 in figure 2 of Gaskins, for example).

Claims 3,8,11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunda et al. (U.S. Patent No. 5,715,476) in view of Ryan (U.S. Patent No. 6,405,280) in further view of Gaskins et al. (U.S. Patent No. 6,081,853) in further view of Kobayashi et al. (U.S. Patent No. 5,394,528).

As per claims 3,8,11, and 18, Kobayashi teaches a bus-sizing function that allows a processor to issue a single bus request instead of multiple requests over smaller external buses (column 7, lines 15-27) when data is to be accessed from main memory, such as in the event of a cache miss (column 3, line 37-39). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to combine the data processing system of Kunda (with cache system represented by Gaskins) with the teaching of the bus-sizing function of Kobayashi in order to have reduced the complexity of the processor in the data processing system by eliminating the need for the internal function circuit of the processor to operate under the control of different procedures for different bus width sizes (column 7, lines 22-26).

As discussed in column 12, lines 17-23 of Kobayashi, a first burst access from a main memory in response to a cache miss (mishit) is accessed in order according to the block address causing the miss (in this case block address x0008) and then wrapping-around the address bounds for the burst, as can be seen by the transition from address x000C to x0000 (column 12, line 20). For a second burst transfer, accessing is performed in linear order starting with the -- top boundary-- as can be seen in column 12, line 22.

Response to Amendment

As per Applicant's amendment filed 3 June 2004, the following Examiner's objections/rejections have been respectfully withdrawn hereto:

(i) The objections to the drawings;

(ii) The objections to claims 1-14;

(iii) The rejections of claims 4-8 and 12-14 under §112, second paragraph;

(iv) The rejections of claims 1,4,5, and 9 under §102(b) as being anticipated by Kundu et al. (U.S. Patent No. 5,715,476);

(v) The rejections of claims 2,6,7,10,12,13, under §103(a) as being unpatentable over Kunda et al. (U.S. Patent No. 5,715,476) in view of Gaskins et al. (U.S. Patent No. 6,081,853);

and (vi) The rejections of claims 3,8,11, and 14 under 35 U.S.C. 103(a) as being unpatentable over Kunda et al. (U.S. Patent No. 5,715,476) in view of Gaskins et al. (U.S. Patent No. 6,081,853) in further view of Kobayashi et al. (U.S. Patent No. 5,394,528).

At present, following the present Office action, claims 1,4,5, and 9 stand rejected under §103(a) as being unpatentable over Kundu et al. (U.S. Patent No. 5,715,476) in view of Ryan (U.S. Patent No. 6,405,280); claims 2,6,7,10,12,13 stand rejected under §103(a) as being unpatentable over Kundu et al. (U.S. Patent No. 5,715,476) in view of Ryan (U.S. Patent No. 6,405,280) in further view of Gaskins et al. (U.S. Patent No. 6,081,853); and claims 3,8,11, and 14 stand rejected under §103(a) as being unpatentable over Kundu et al. (U.S. Patent No. 5,715,476) in view of Ryan (U.S. Patent No. 6,405,280) in further view of Gaskins et al. (U.S. Patent No. 6,081,853) in further view of Kobayashi et al. (U.S. Patent No. 5,394,528).

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

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